

# **Synopsis V1.0 Gflx Qchip test vehicle TID TEST REPORT**

Christian Poivey<sup>1</sup>, Jim Forney<sup>1</sup>

<sup>1</sup>Muniz Engineering, Inc.

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## **1 Introduction**

This report presents the total ionizing dose (TID) testing results of the logic chip (Qchip) test vehicle of LSI Logic Gflx standard process and two radiation-enhanced versions of this process. This work was performed in the frame of NASA NEPP program.

## **2 Tested parts**

LSI Logic Gflx standard technology is a 0.11  $\mu\text{m}$  CMOS bulk process. The two versions of the radiation-hardened process include a buried layer in order to guarantee SEL immunity.

The Logic chip test vehicle L9A0443 contains 384 64-bit ALU and 4 PRMNDM3 (process monitor) organized as 6 64 64-bit ALU modules (ALU\_64\_HD). In each module, the 64 ALUs share the same inputs and the output pass through a 64:1 output MUX tree. Each ALU (ALU\_WRAP\_HD) has a scan chain that connect the 200 flip-flop (operands a and b, outputs,...). Individual ALU outputs are only accessible through the scan chain. The power supply core voltage is 1.2V, and the I/O supply voltage is 3.3V. The Logic test vehicle is packaged in a cavity up 492 PBGA package (code I735).

Four parts were irradiated. One additional device per test vehicle served as control sample. Tables 1 gives the package marking and the serial number of test samples.

Table 1: test samples

Test vehicle	Process	Marking	SN#
L9A0443	Standard (bulk)	LSI Logic L9A0492 GAH15900.14 EEH27001.1 Control 24 G 0528 Δ Korea	1
	Buried layer 1 (Dose 5)	LSI Logic L9A0492 GAH15900.14 EEH27001.3 1.6M5E14 12 G 0528 Δ Korea	33, 36
	Buried layer 2 (Dose 1)	LSI Logic L9A0492 GAH15900.14 EEH27001.2 1.6M1E14 7 G 0528 Δ Korea	17

### 3 Test Method

Test samples were exposed using the NASA GSFC Co<sup>60</sup> source per MIL-STD-883 Method 1019.6. The dose levels were 10, 40, 110, 160, 210, and 310 krad-Si at a dose rate between 200 and 18000 rad-Si/hour. The detail of the irradiation test sequence is given in appendix 1.

At each dose level all test samples, including the control parts, were be characterized using the parametric measurements given in Table 2. During exposure the devices are biased in scan mode at nominal supply voltage and a clock frequency of 1 MHz with an alternate input pattern.

Table 2. Parametric Characteristics (Vcore=1.2V, VI/O=3.3V)

Parameter	Condition	Units
Functional test	Alternate pattern, 1MHz	
Vdd core Power supply dynamic current	Alternate pattern, 1MHz	mA
Vdd core Power supply standby current	No clock	mA
VI/O Power supply dynamic current	Alternate pattern, 1MHz	mA
VI/O Power supply standby current	No clock	mA

#### 4 Results

Test results did not show any functional failure or degradation up to the maximum test dose of 310 krad-Si. Fig. 1 to 3 show core and I/O supply currents in function of total dose.

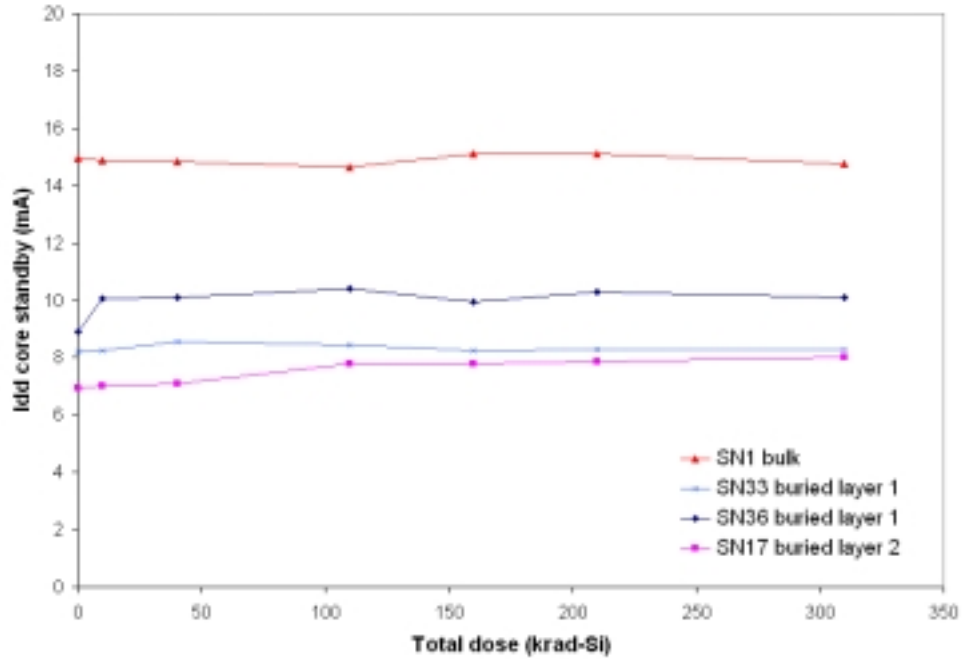


Fig. 1: Idd core standby current versus total dose

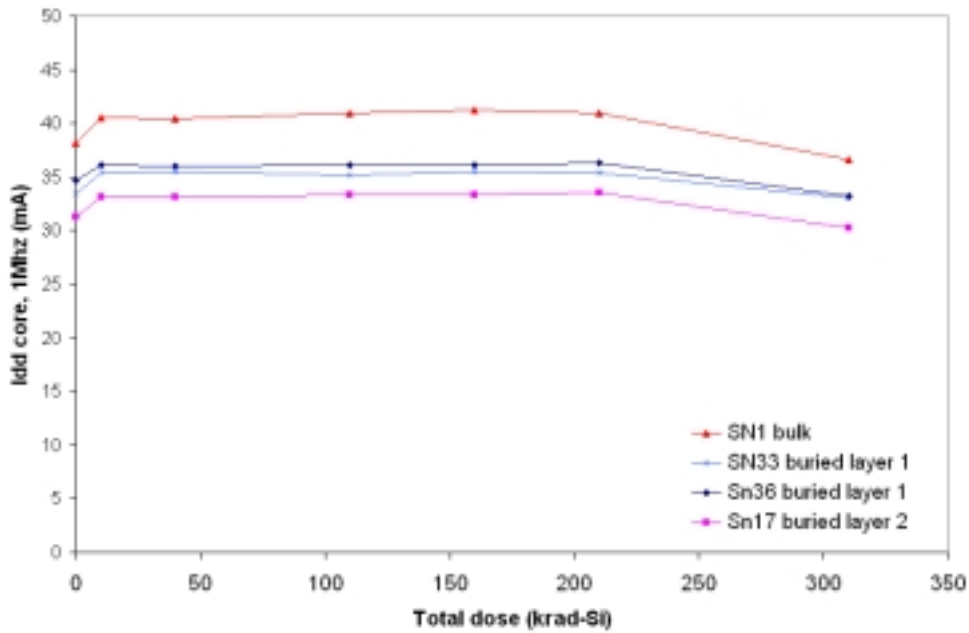


Fig. 2: Idd core dynamic current at 1MHz versus total dose

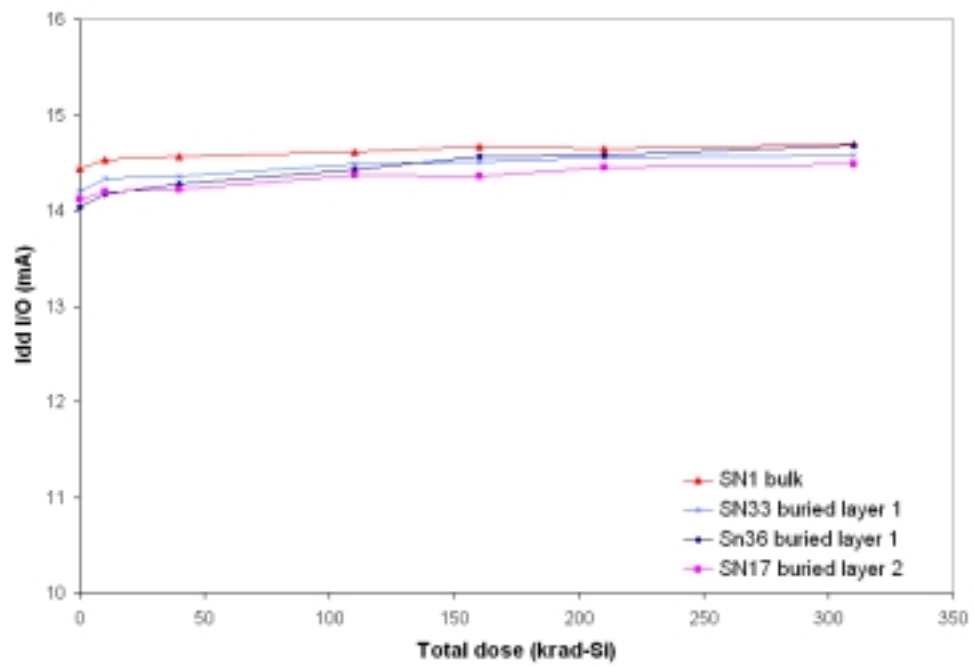


Fig. 3: I/O current (dynamic and static) versus total dose

**Appendix 1: irradiation test sequence**

Step #	Date and Time in		Date and Time out		Description	Exposure Time (h)	dose rate (rad[Si]/mn)	step dose (krad [Si])	Total dose (krad [Si])
0					Initial Elect. Measurements				
1	11/18/05	15h03	11/18/05	16h24	Irradiation	1.35	126.5	10	10
1a	11/18/05	16h24	11/18/05	16h52	Electrical Meas.				
2	11/18/05	16h52	11/21/05	11h00	Irradiation	66.13	10.1	40	50
2a	11/21/05	11h00	11/21/05	11h53	Electrical Meas.				
3	11/21/05	11h53	11/22/05	10h35	Irradiation	22.7	44.025	60	110
3a	11/22/05	10h35	11/22/05	12h01	Electrical Meas.				
4	11/22/05	12h01	11/22/05	14h49	Irradiation	2.83	296.5	50	161
4a	11/22/05	14h49	11/22/05	15h38	Electrical Meas.				
5	11/22/05	15h38	11/23/05	11h02	Irradiation	19.4	42.875	50	211
5a	11/23/05	11h02	11/23/05	11h56	Electrical Meas.				
6	11/23/05	11h56	11/25/05	12h14	Irradiation	48.3	34.45	100	310
6a	11/25/05	12h14	11/25/05	13h00	Electrical Meas.				